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Roll No. :

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B. E. (Third Semester) Examination, Nov.-Dec. 2021

(New Scheme)

(IT Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : Attempt all questions. Part (a) from each question is compulsory and carry 2 marks. Attempt any two parts (b), (c) & (d) with carries 7 marks each.

Unit-I

1. (a) Convert $[5497]_{10}$ to Binary. 2
- (b) Solve the following using Tabulation (Quine-McCluskey) method : 7

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[2]

$$F(A, B, C, D) = \sum(0, 1, 5, 7, 8, 10, 14, 15)$$

(c) Solve this using K Map : 7

(i) $F(A, B, C, D) = \pi M(1, 5, 6, 7, 11, 12, 13, 15)$

(ii) $F(A, B, C, D) = \sum m(1, 5, 6, 12, 13, 14)$
 $+ d(2, 4)$

(d) Write short notes on the following : 7

- (i) NAND & NOR gates as a Universal Gate
(ii) Demorgan's Theorem

Unit-II

2. (a) Explain term Fan-in & Fan-out. 2

(b) Explain two input TTL NAND Gate with proper diagram & I/O characteristics. 7

(c) Explain I^2L NAND & NOR Gate with diagram. 7

(d) Explain CMOS AND Gate. 7

Unit-III

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3. (a) Design a full Adder with its table. 2

(b) Design a look Ahead Carry generator with its diagram & expression. 7

(c) Design a 32×1 Multiplexer using 8×1 Multiplexer. 7

(d) Design a 4 bit BCD – Gray Code Convertor. 7

Unit-IV

4. (a) Consider a 4-bit Johnson counter with an initial value of 0000. What is counting sequence of this counter. 2

(b) Design a counter using J K Flip Flop that goes through state 3, 4, 6, 7 and 3 Is the counter is self starting? Modify the circuit such that whenever it goes to an invalid state it comes back to state 3. 7

(c) Design a 4 Bit Ring Counter with starting sequence 1000. 7

(d) Explain Master Slave J-K Flip Flop. 7

Unit-V

5. (a) What is a Sequential Machine? 2

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(b) Explain the differences between Mealy & Moore Machine with proper a example & its state diagram. 7

(c) Solve this using PLA :

$$F1(A, B, C) = \sum m(3, 5, 6, 7)$$

$$F2(A, B, C) = \sum m(0, 2, 4, 7) \quad 7$$

(d) Explain the PAL with example & proper diagram. 7